**Design Lab Report**

For my design lab, I chose to do a digital lock. The lock takes in inputs from four different pushbuttons, and displays the output on the 7 segment display. Before being able to take in any pushbutton inputs, I made it so that there is a switch enable. If the enable switch is not on, it does not matter if you enter the correct combination, it will not unlock. This was decided because perhaps you do not want to unlock the lock, but somehow the buttons were pressed in the proper order. Though this is unlikely, it would be even more unlikely to have a switch flipped and all the buttons pushed in the order.

Based on the wanted output of my design, and after talking with Dave, I chose to go with state-based design. I believe this is the best design because I wanted the pushbutton sequence to be what determines whether it is locked or unlocked. State-based design makes sure to not leave the state and continue to the next if the proper sequence is not inputted. Therefore, even if the user inputs 3 out of 4 of the buttons in the correct sequence, the lock will go back to the initial state and the user should have to restart the sequence. The lock involves four pushbuttons needing to be pressed in order for the lock to open. This is done by looking to see if the first button was pressed it while the state is in all 0’s, “0000”. Once the button is pushed it will then change the state to “0001” and move to the next state to be looked at and so forth. As for the 7 segment display, the display will show an “L” for “Locked” at all times other than when the pushbuttons are pushed in the proper order, changing this “L” to a “U” for “Unlocked”. This is done by an active low design with a common anode display. Therefore, when wanting to change the letters, you would input different cathode values. Once the 7 segment display goes into the unlocked state, it remains there until the program is reloaded onto the board.

I left my project like this because creating a reset on the board would be fairly easy, however, unnecessary and would be wasting my time. In the end this project wasn’t too difficult and was actually a good lab to introduce myself to state-based design in VHDL.